FIG. 1A

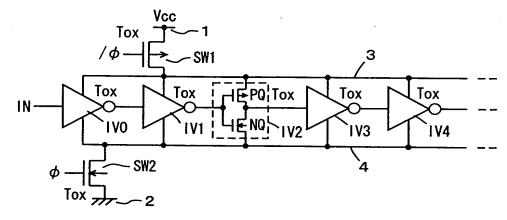


FIG. 1B

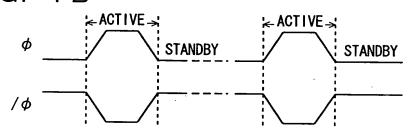


FIG. 2A

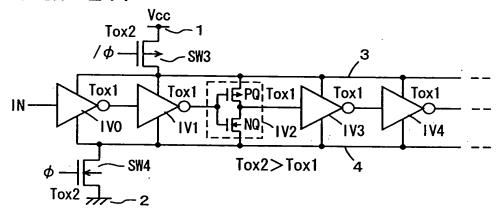


FIG. 2B

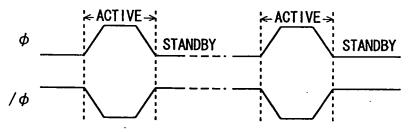


FIG. 3A

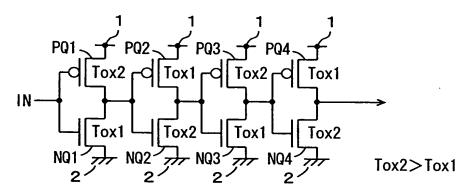
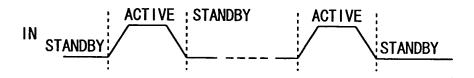
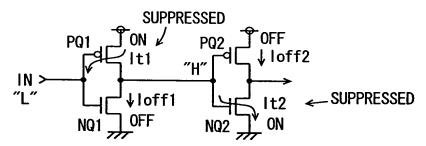
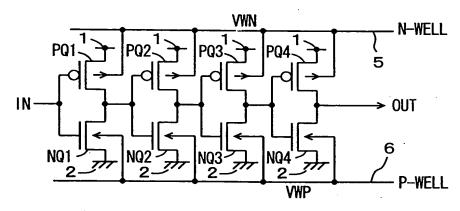


FIG. 3B

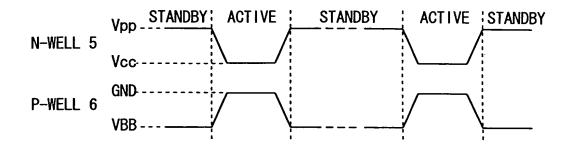


F I G. 4





F I G. 6



F I G. 7

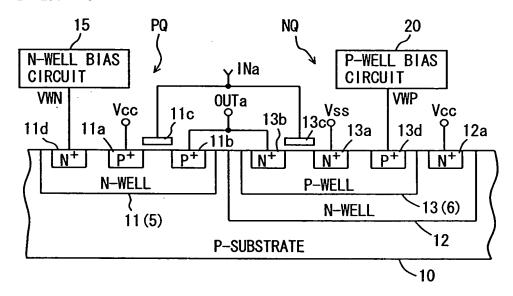


FIG. 8A

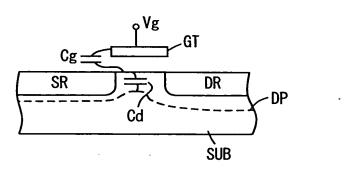


FIG. 8B

Cg

Cd

ა. Vsub

FIG. 9

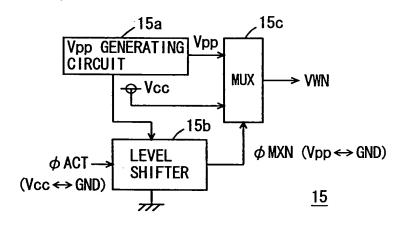
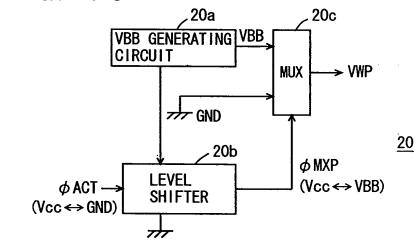
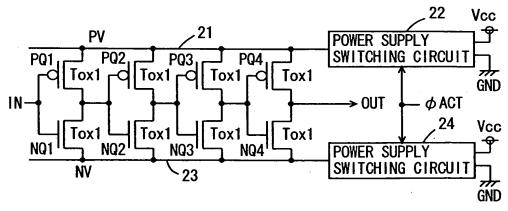
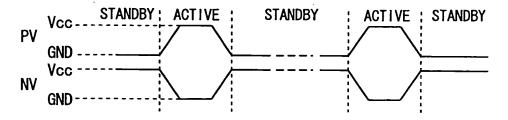


FIG. 10



F I G. 11





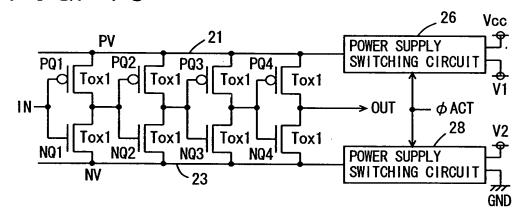


FIG. 14

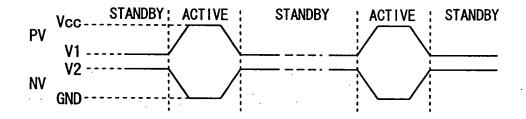
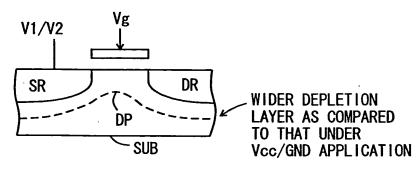
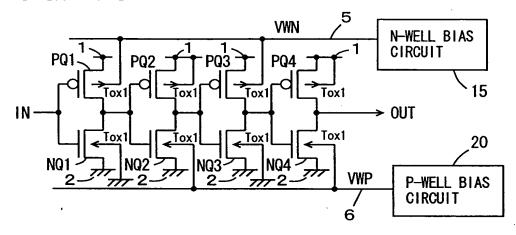


FIG. 15





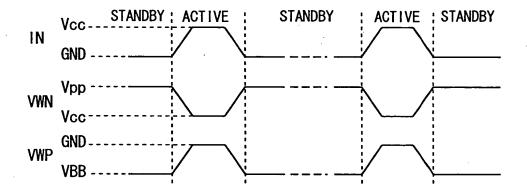


FIG. 18

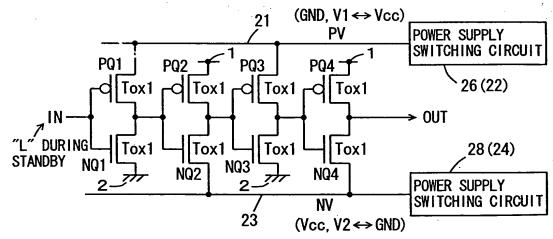


FIG. 19

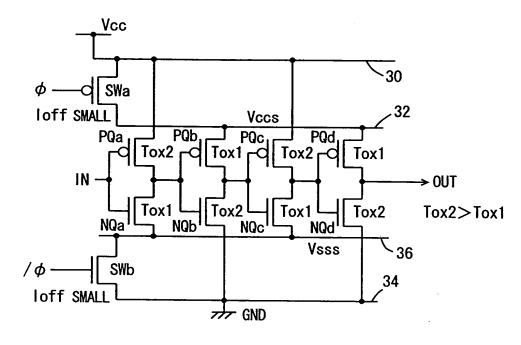


FIG. 20

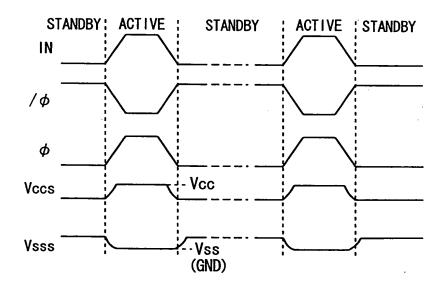


FIG. 21A G SWa, b SUa, b SWa, b SUa, b SUa,

FIG. 22

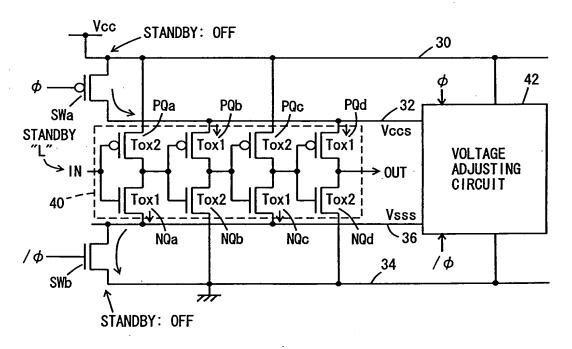


FIG. 23

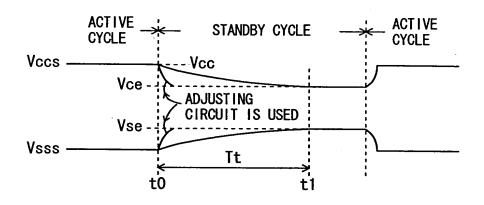
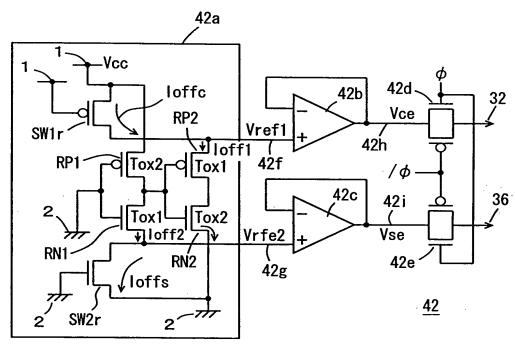


FIG. 24



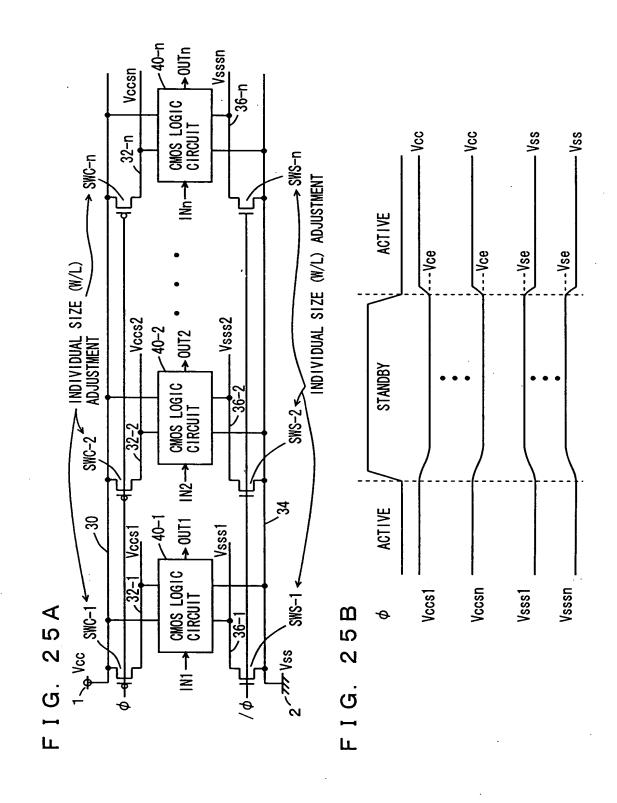
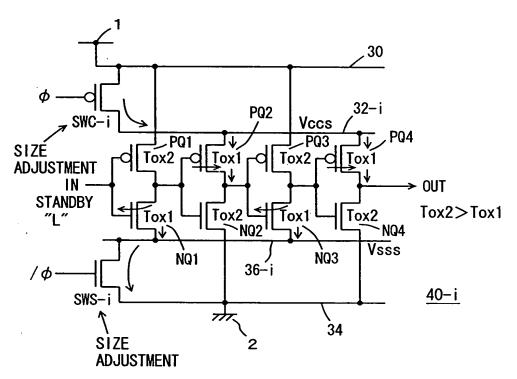


FIG. 26



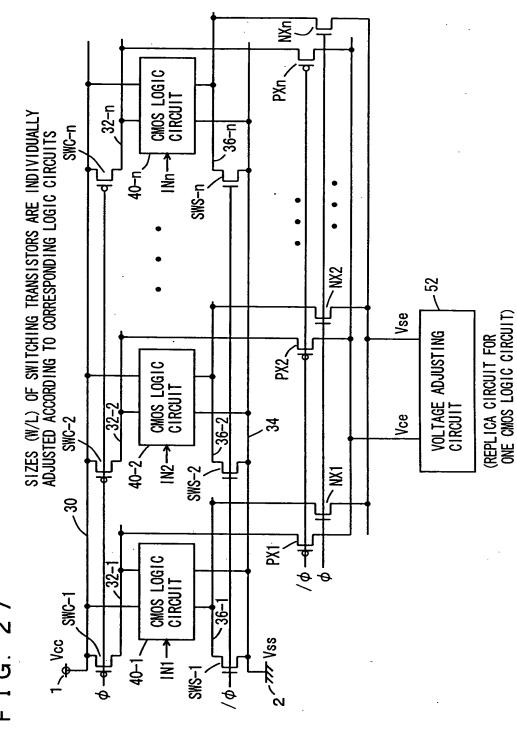
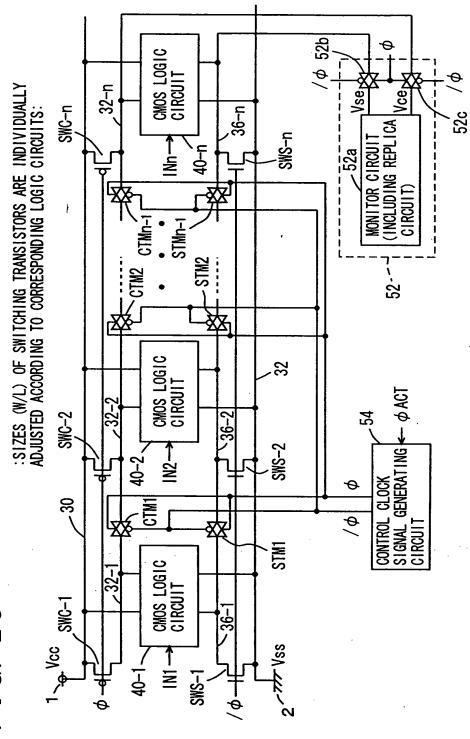


FIG. 27

CMOS LOGIC CIRCUIT 32-n :SIZES (W/L) OF SWITCHING TRANSISTORS ARE INDIVIDUALLY ADJUSTED ACCORDING TO CORRESPONDING LOGIC CIRCUITS: SWC-n 36-n SWS-n <u>↑</u> STMn-1 CTM2 CMOS LOGIC CIRCUIT CONTROL CLOCK
SIGNAL GENERATING - ϕ ACT
CIRCUIT 32-2 SWC-2 **√36-2** 54 SWS-2 40-2 P 8 CTM1 φ/ STM CMOS LOGIC CIRCUIT SWC-1 36-1 1 Vcc 2 mr Vss ↑ ≥ 40-1 SWS-1 中 **-**φ/

FIG. 28



F I G. 29

FIG. 30

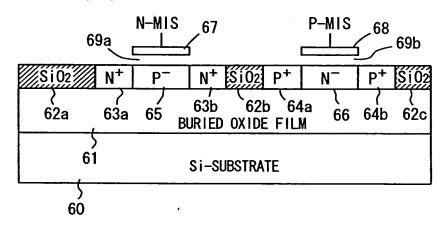


FIG. 31A

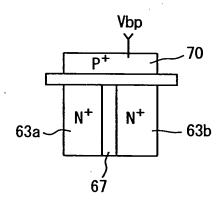


FIG. 31B

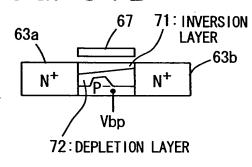


FIG. 32

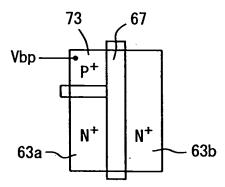


FIG. 33A

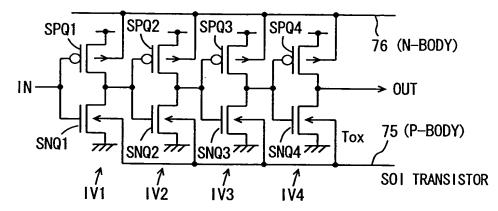


FIG. 33B

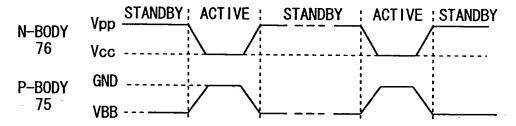


FIG. 34A

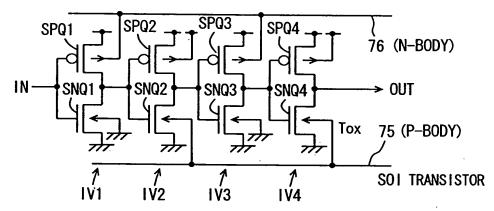


FIG. 34B

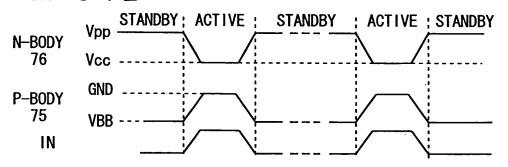


FIG. 35

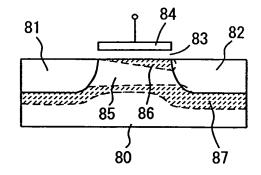


FIG. 36A

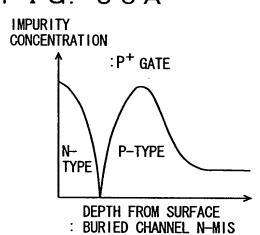


FIG. 36B

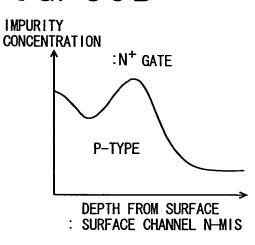


FIG. 37A

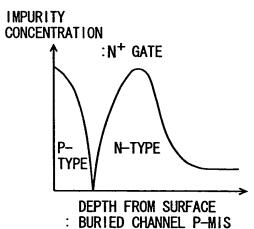


FIG. 37B

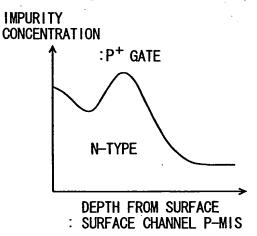


FIG. 38A B01 + P02 + B03 + P04 + F0x1 rd Tox1 rd Tox1 → 0UT Tox1 Tox1 NQ1 777 BQ2 777 NQ3 777 BQ4 FIG. 38B : ACTIVE : STANDBY . ACTIVE . STANDBY FIG. 39A - Vcc SWa loff SMALL Vccs BQa PQb BQc PQd Tox1 → 0UT Tox1 BQd Tox1 | Tox1 | NQc Tox1 ⁷36 Vsss $/\phi$ SWb 34 loff SMALL J GND FIG. 39B STANDBY: ACTIVE : **STANDBY** : ACTIVE : STANDBY IN φ

 $/\phi$

F I G. 40A

FIG. 40B

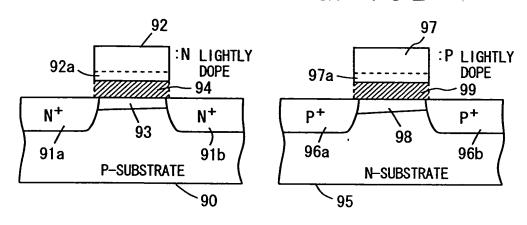


FIG. 41

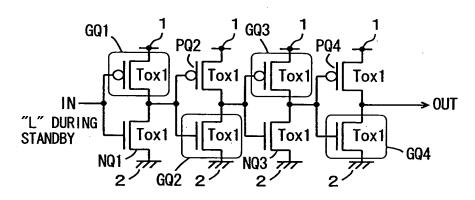


FIG. 42

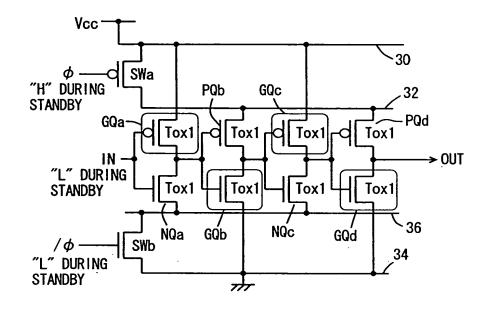


FIG. 43

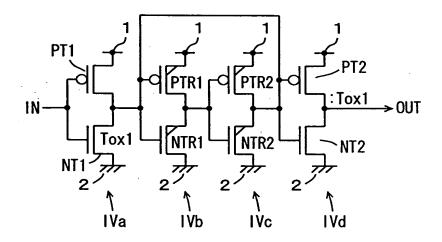


FIG. 44

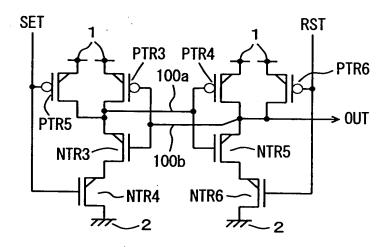


FIG. 45

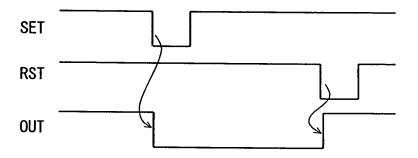


FIG. 46

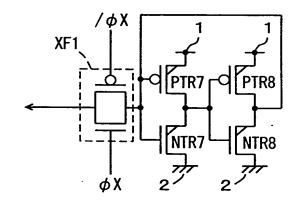


FIG. 47

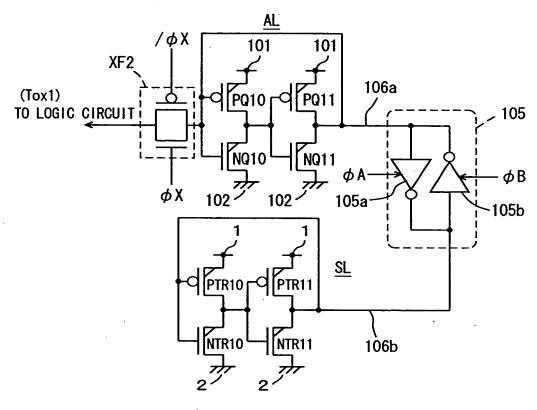


FIG. 48

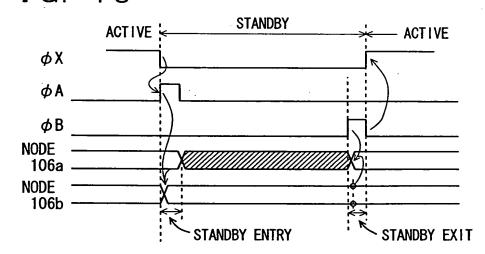


FIG. 49A

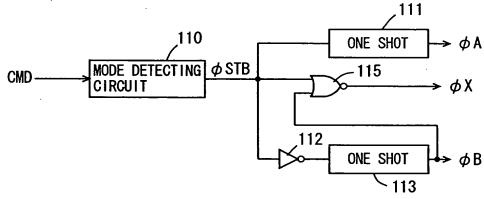


FIG. 49B

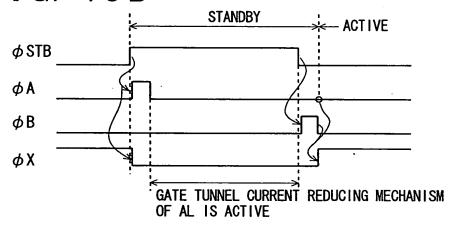


FIG. 50

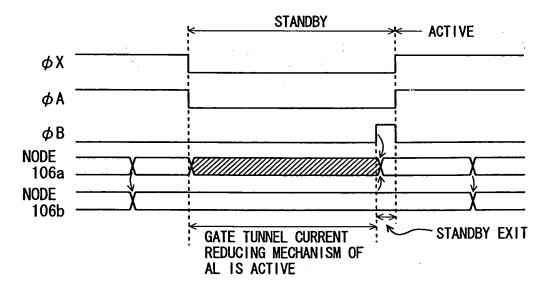


FIG. 51A

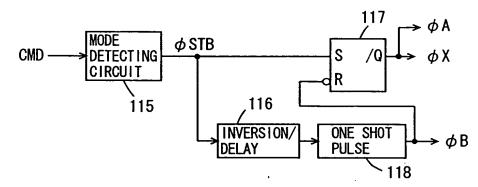


FIG. 51B

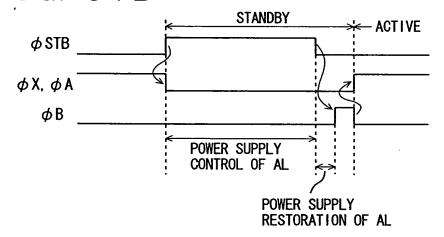


FIG. 52

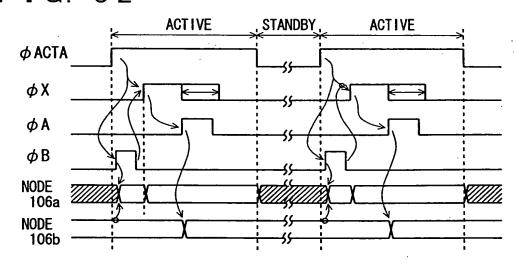


FIG. 53

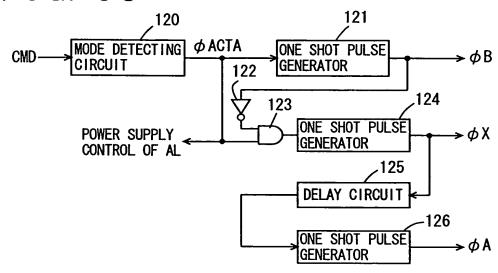
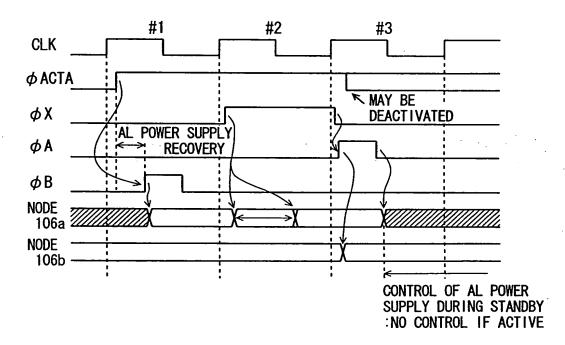


FIG. 54



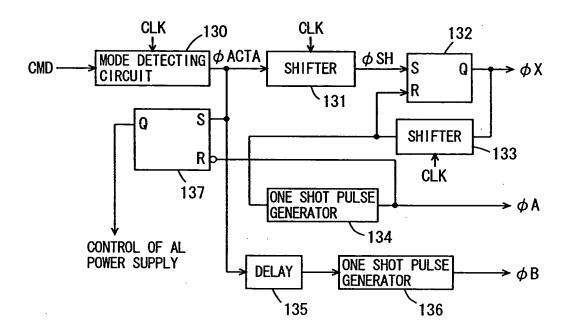


FIG. 56A

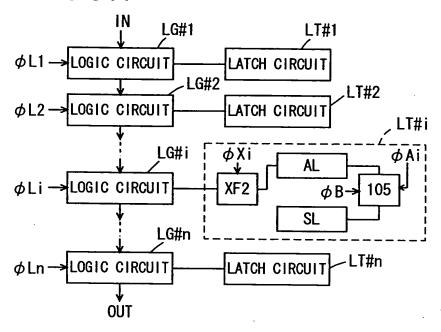


FIG. 56B

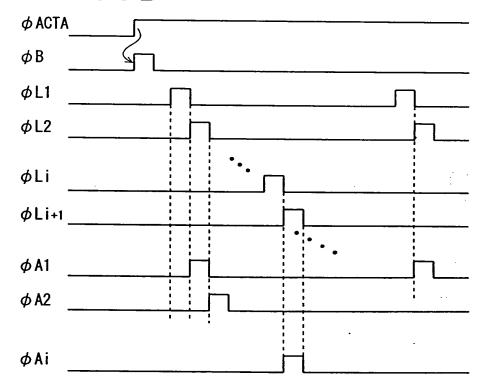


FIG. 57A

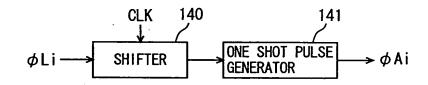
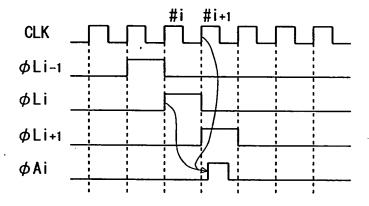


FIG. 57B



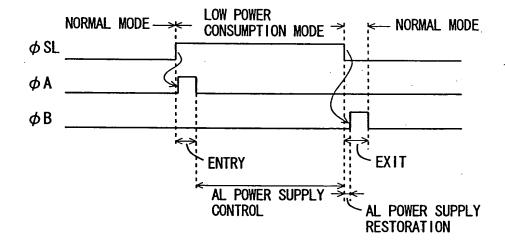


FIG. 59A

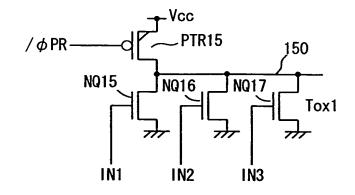


FIG. 59B

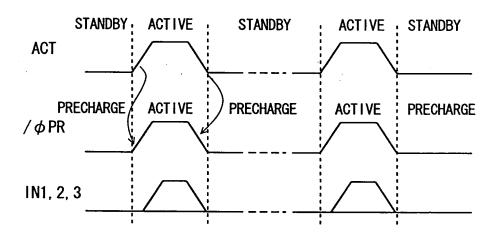


FIG. 59C

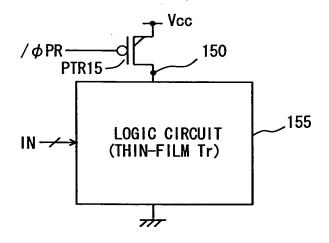


FIG. 60A

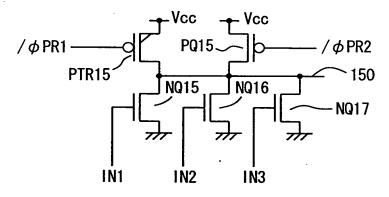


FIG. 60B

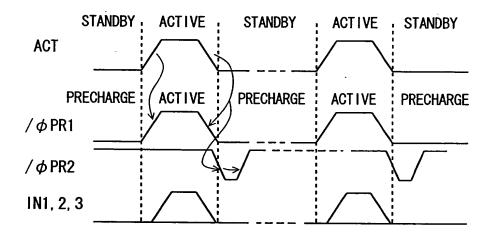
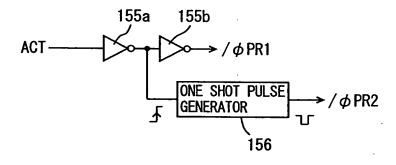


FIG. 61



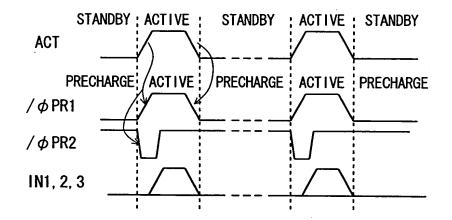
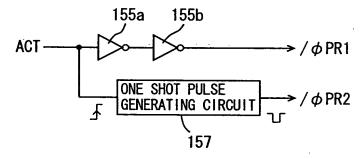


FIG. 63



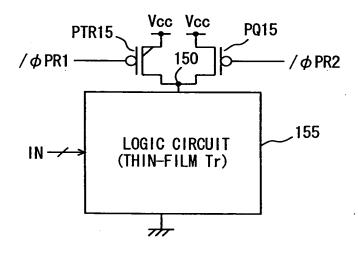


FIG. 65

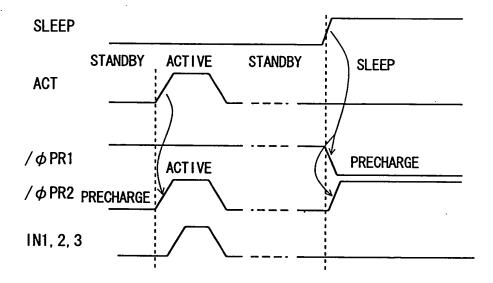


FIG. 66

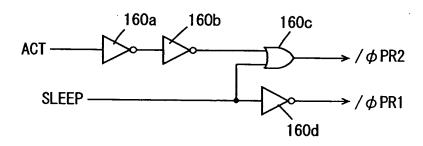


FIG. 67A

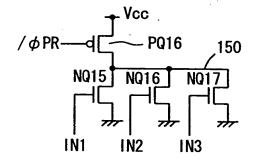
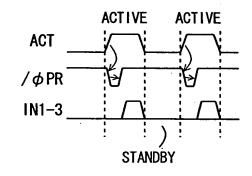


FIG. 67B



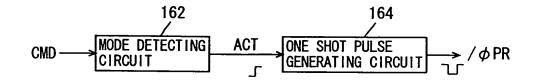
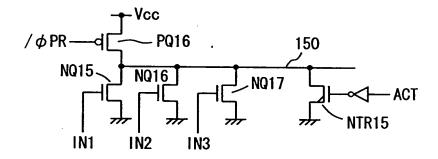


FIG. 69



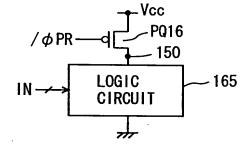
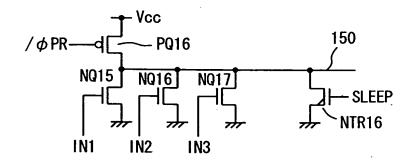
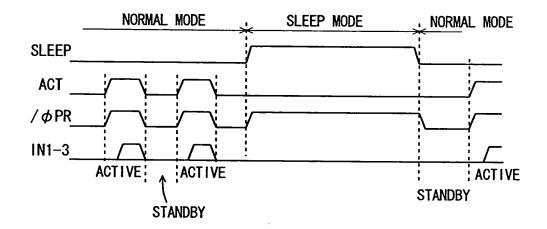


FIG. 71





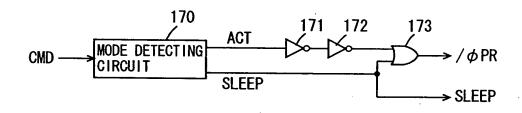


FIG. 74A

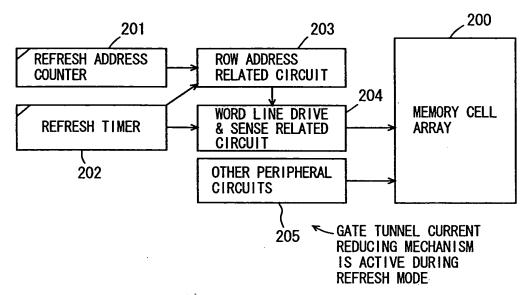


FIG. 74B

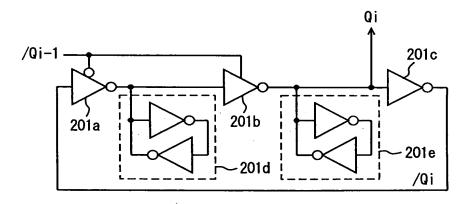


FIG. 75

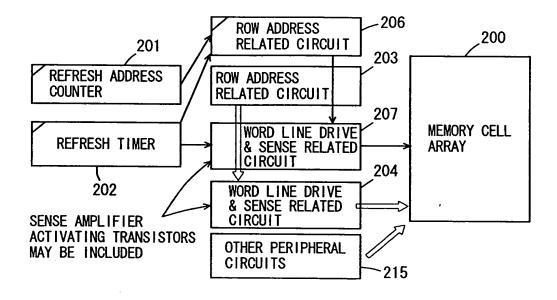


FIG. 76

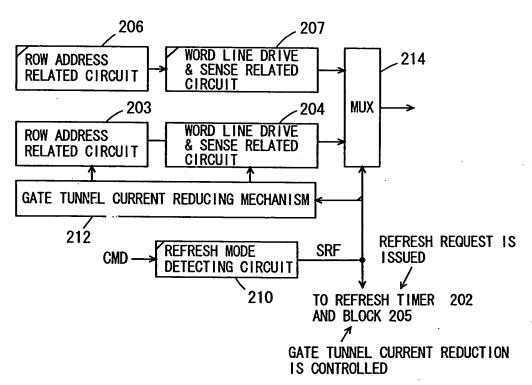


FIG. 77

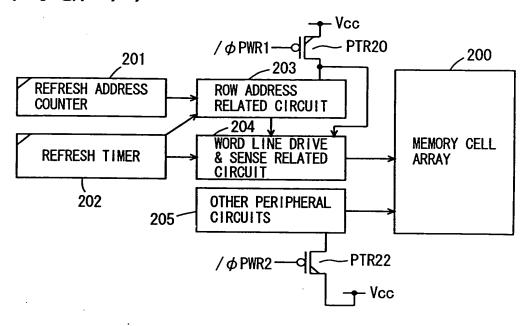


FIG. 78

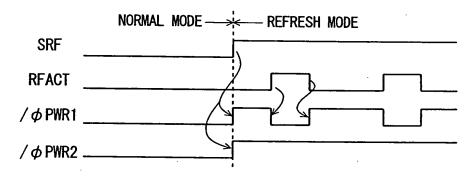


FIG. 79

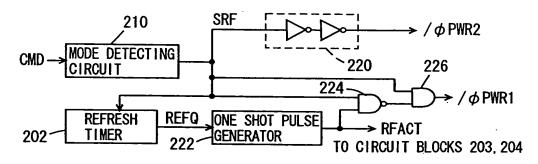


FIG. 80

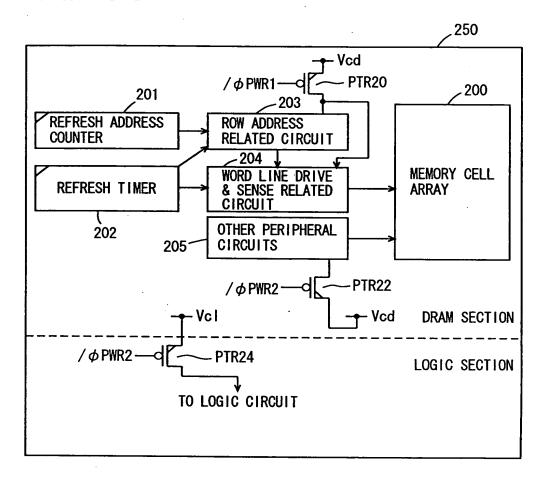


FIG. 81

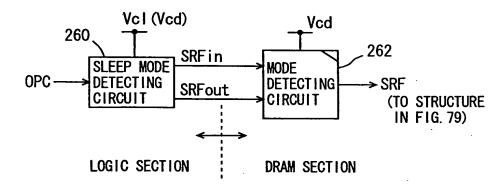


FIG. 82

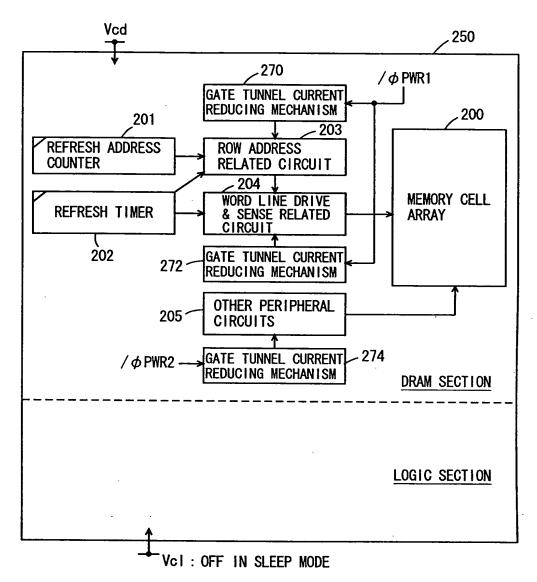


FIG. 83

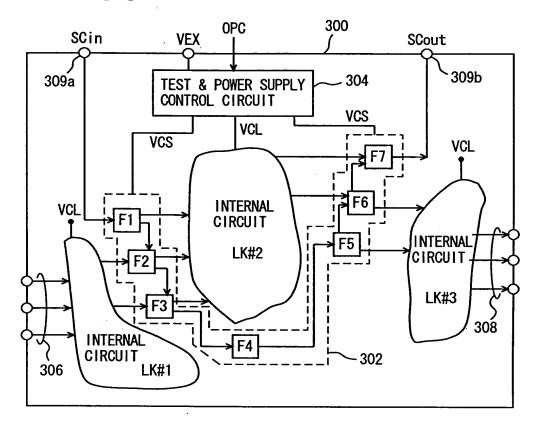


FIG. 84

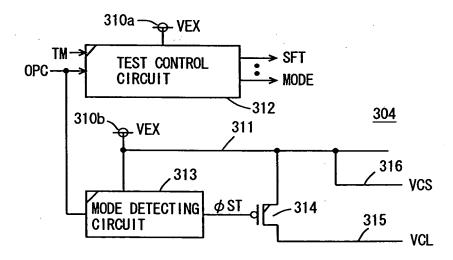


FIG. 85

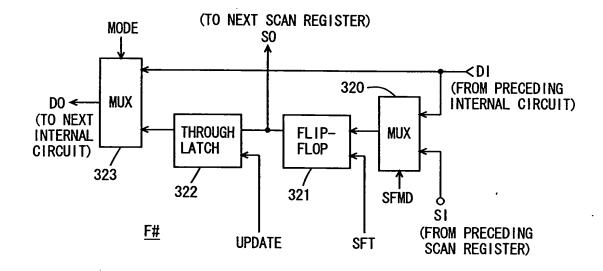


FIG. 86

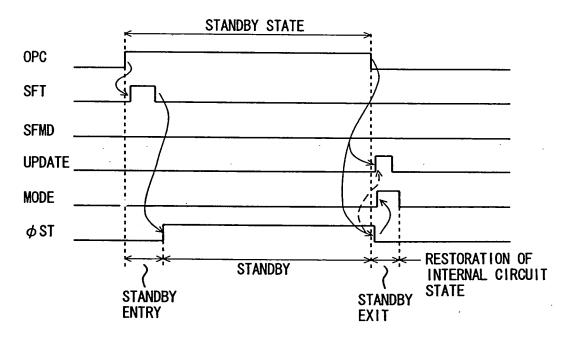


FIG. 87

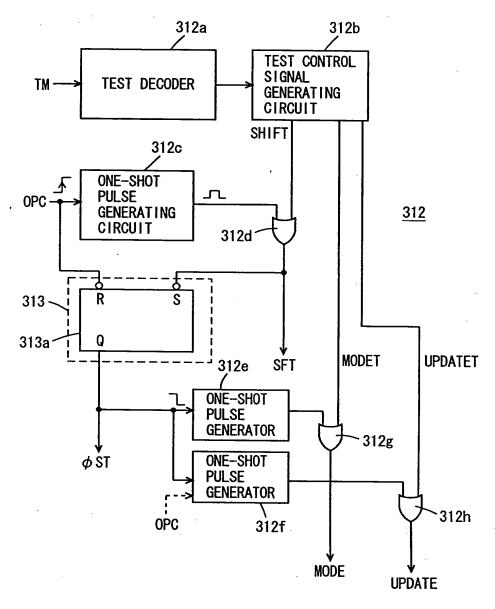


FIG. 88

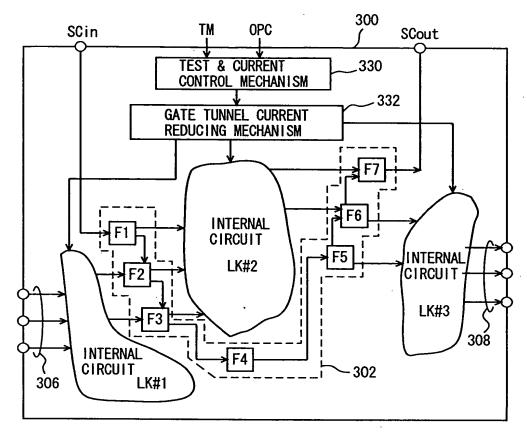


FIG. 89

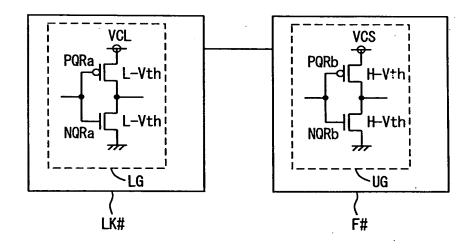


FIG. 90

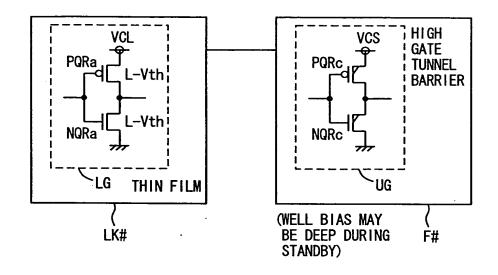


FIG. 91

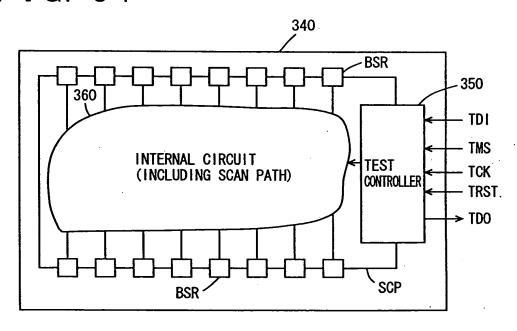


FIG. 92

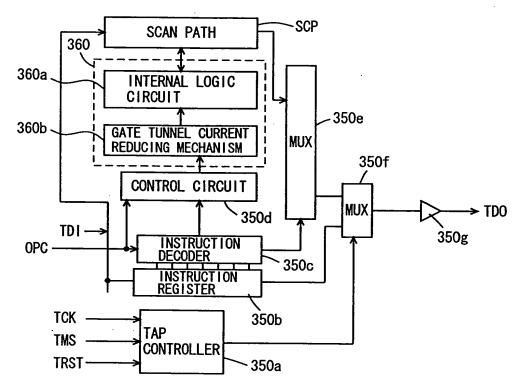
FIG.

93

416

CIRCUITS

OTHER PERIPHERAL



402 404 406 CB#1 CB#2 CB#n 400 **RB#1 RB#2** WORD **ROW** LINE **ADDRESS** ROW DRIVE & INPUT DECODER SENSE-CIRCUIT RELATED CIRCUIT

410

CIRCUIT

COLUMN DECODER

COLUMN ADDRESS INPUT

_ RB#m

408

DATA 10

CONTROL

412

FIG. 94

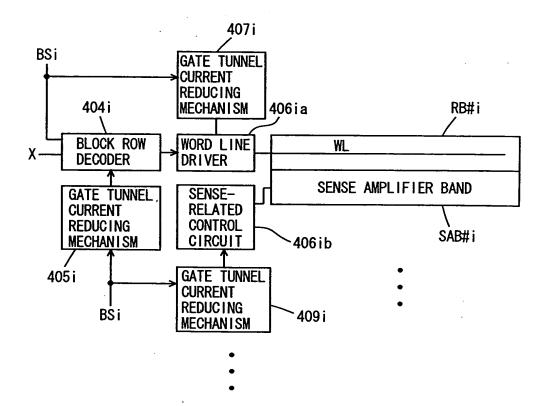


FIG. 95

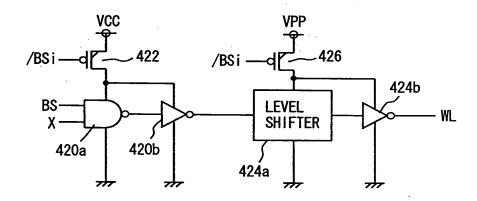


FIG. 96

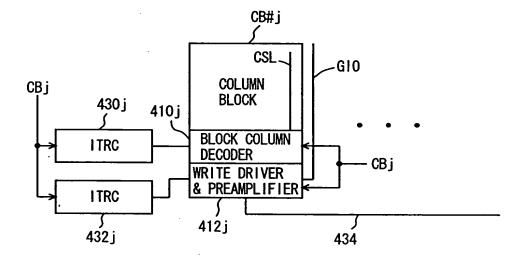


FIG. 97

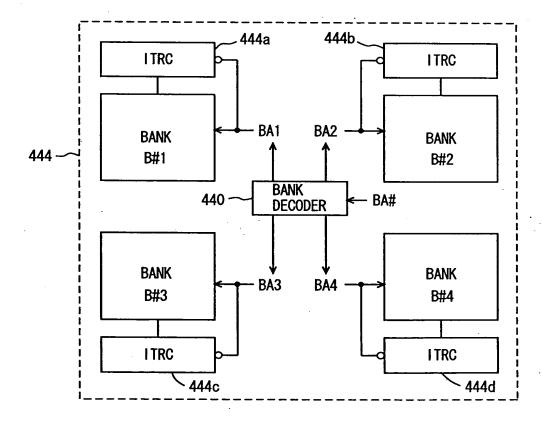


FIG. 98

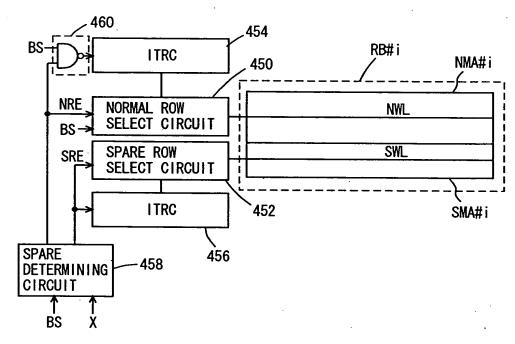


FIG. 99

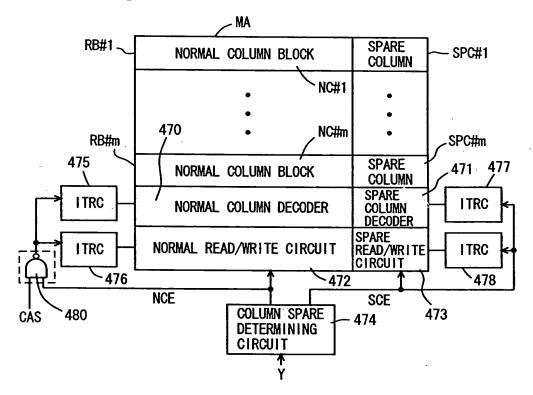
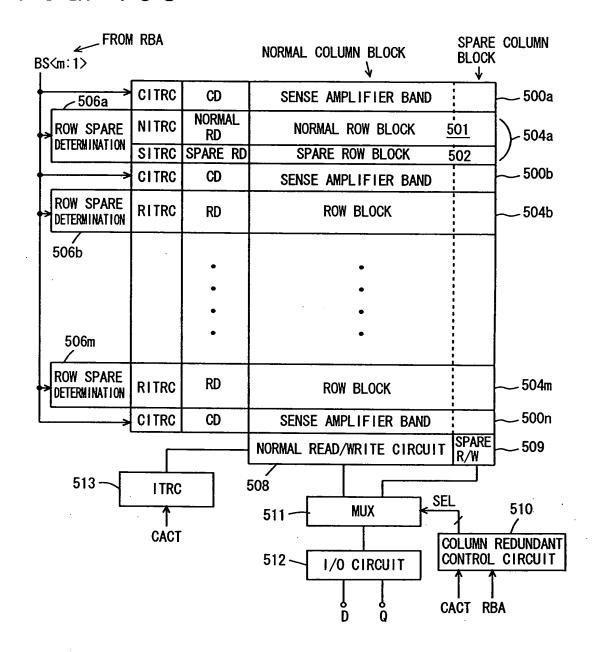
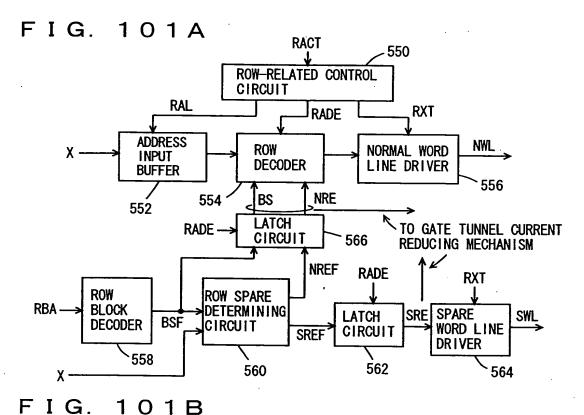
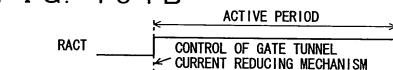


FIG. 100







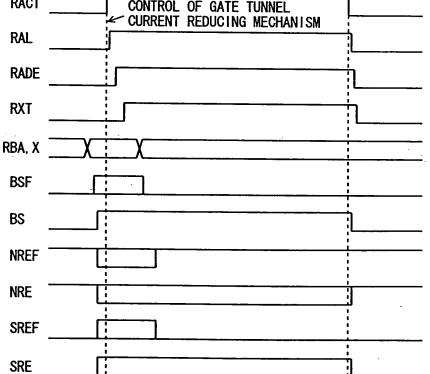


FIG. 102

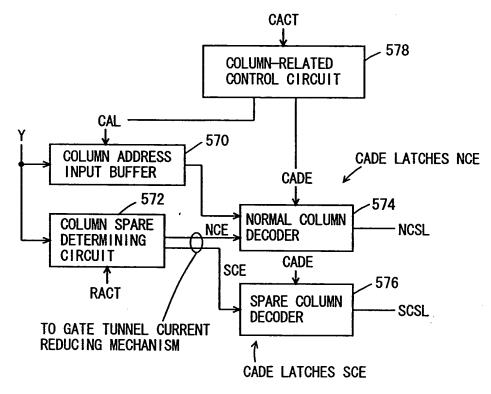


FIG. 103

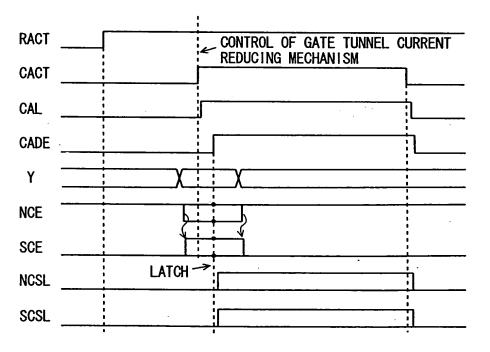


FIG. 104 PRIOR ART

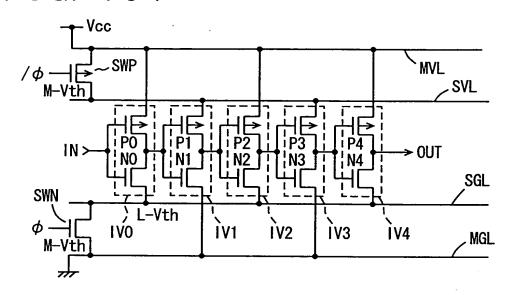


FIG. 105 PRIOR ART

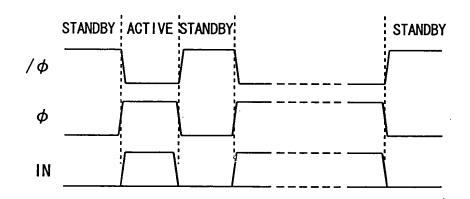


FIG. 106A PRIOR ART

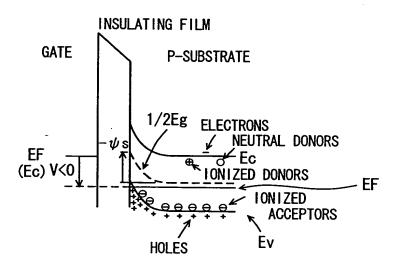


FIG. 106B PRIOR ART

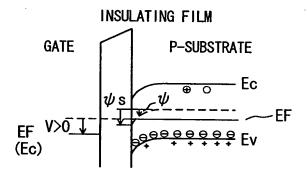


FIG. 106C PRIOR ART

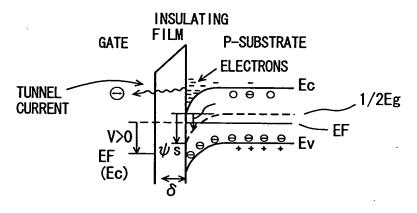


FIG. 107 PRIOR ART

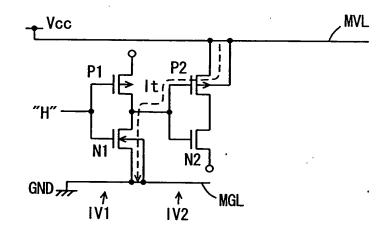


FIG. 108 PRIOR ART

